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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 09/966,095
Filing Date: October 01, 2001
Appellant(s): BALAY ET AL.

Bollman
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 12/21/2005 appealing from the Office action mailed 6/2/2005.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

**(9) Grounds of Rejection**

The following grounds of rejection are applicable to the appealed claims:

At the outset, it is noted that the statutory basis for the rejection remains the same, and no new prior art is relied upon. The following changes have been made in rejections:

The 35 USC 103 rejection over Nakamura is hereby withdrawn because of redundancy and in order to reduce the issues presented to the Board of Appeals. However, under 37 CFR 1.196(b), the Board may, in its decision, reintroduce 35 USC 103 rejection of the claims over Nakamura.

**The Tal 103 Rejection:**

Old:

Broader independent claims 1, 10, and 19 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Tai.

Narrower dependent claims 7, 16, and 25 (depending from claims 1, 10, and 19, respectively, has been rejected under 35 U.S.C. 103(a) as being unpatentable over Tal in view of old well-known prior art such as the Applicants' acknowledged prior art, Lattice Semiconductor Corp., and Lucent Technologies.

New:

Broader independent claims 1, 10, and 19 as well as their narrower dependent claims 7, 16, and 25 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Tal in view of Lucent Technologies.

**The Lange 103 Rejection:**

Old:

Broader independent claims 1, 10, and 19 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Lange.

Narrower dependent claims 7, 16, and 25 (depending from claims 1, 10, and 19, respectively, has been rejected under 35 U.S.C. 103(a) as being unpatentable over Lange in view of old well-known prior art such as the Applicants' acknowledged prior art, Lattice Semiconductor Corp., and Lucent Technologies.

New:

Broader independent claims 1, 10, and 19 as well as their narrower dependent claims 7, 16, and 25 are now rejected under 35 U.S.C. 103(a) as being unpatentable over Lange in view of Lucent Technologies.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6- 8, 10-12, 15-17, 19-21, 24- 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tal in view of Lucent Technologies.

With regard to claim 1, Tal discloses a system for interconnectlng two or more computer bus architectures (the compact PCI (Peripheral Component Interconnect) shown generally at Fig. 8, for example), comprising: a first bus segment (PCI bus segment 802, column 6, lines 43-64, for example) to transmit data information, a first half bridge circuit (the PCI serializer on system card 810 in segment 802, Fig. 8, and shown in details as PCI serilalizer 700 on segment 802, Fig. 7, column 6, lines 28-38; note that the extra serializer in card 806 on PCI bus segment 802, showed in Fig. 8, are only for redundancy; note also that the circuit 700, Fig. 7, corresponds to the half bridge disclosed by the Applicant in the originally filed specification, page 1, lines 12-17; page 6, lines 20-26, page 7, line 1 to page 9, line 4; and particularly Fig. 2.) connected to said first bus segment (PCI bus segment 802, column 6, lines 43-64, for example), said first half bridge circuit (PCI serializer 700, shown at Fig. 7, on segment 802 side, Fig. 8) comprising a first DMA circuit (704, Fig. 7, column 6, lines 28-28); a second bus segment (PCI bus segment 804, column 6, lines 43-64, for example) to transmit data information; a second half bridge circuit (the PCI serializer on card 812 in segment 804, Fig. 8, and shown in details as PCI serilalizer 700 on segment 804, Fig. 7, column 6, lines 28-38; note that the extra serializer in card 808 on PCI bus segment 804, showed in Fig. 8, are only for redundancy) connected to said first half bridge circuit (700, shown at Fig. 7, on segment 802 side), said second half bridge circuit (700, shown at Fig. 7, on segment 804 side) comprising a second DMA circuit (704, Fig. 7) and transferring data

information between said first bus segment (segment 802, column 6, lines 43-64, for example), and said second bus segment (segment 804, column 6, lines 43-64, for example). Tal further discloses that the serial channel (having a plurality of data paths connecting the first half bridge to the second half bridge) is built out of 4 full duplex pairs, each providing 622 mbps of bandwidth. See column 6, lines 18-27. As disclosed by the Applicants in the originally filed specification, page 6, lines 5-8, and lines 20-26, "the first half bridge circuit 4 is connected with the second half bridge circuit 6 by four full duplex high speed serial data lines 5 each having a bandwidth of 622 Mb/s" (emphasis added).

However, Tal does not disclose that the serial channel comprising 4 full duplex pair can be "scalable" depending on a bandwidth needed for a particular application. To define the term "scalable", Applicants cited page 10, lines 6-10 of originally filed specification, which states that "[a]lthough the present invention is described with reference to embodiments teaching four high speed serial data lines running between two half bridge circuits, the principles of the present invention are equally applicable to the addition or subtraction of high speed serial data lines depending upon the bandwidth needed between two half bridge circuits." See Appeal Brief, Summary of the Invention, last three lines.

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility,

functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 700 (Figs. 7 and 8) on each side of the PCI bus segments of Tal, for the purpose of providing Tal with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs.

With regard to claim 2, it is clear that segment 802 is a PCI architecture bus.

With regard to claim 3, it is clear that segment 804 is a PCI architecture bus.

With regard to claim 6, the first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

With regard to claims 7, 16, and 25, the ORT4622 half bridge includes field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and 4th paragraph.

With regard to claim 8, the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment (see at least column 6, lines 52-64). In any event, since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ (see page 6, lines 20-26), it is clear that the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

With regard to claims 10-12, 15-17, see discussion above regarding claims 1-3, 6, and 8.

With regard to claims 19-21, 24-26, see discussion above regarding claims 1-3, 6, and 8.

Claims 5, 14, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tal, as applied to claims 1-3, 6- 8, 10-12, 15-17, 19-21, 24- 26 above, and further in view of the following.

Tal, as discussed above, discloses the claimed invention. Tal does not disclose that the bus operating frequencies of PCI bus segment (802) and PCI bus segment (804) may be different. However, the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al. Lange clearly discloses that the bridge (PCI bridge connected to PCI buses according to PCI specification) can have a bus width of either 32 bits or 64 bits. See at least column 3, lines 54-60. According to the PCI specification, PCI is operated at 33 MHz using a 32-bit-wide path; and the speed can be increased from 33 MHz to 66 MHz and the bit count can be doubled to 64. Currently, PCI-X provides for 64-bit transfers at a speed of 133 MHz.

| Bus Type | Bus Width | Bus Speed | MB/sec |
|---|---|---|---|
| ISA | 16 bits | 8 MHz | 16 MBps |
| EISA | 32 bits | 8 MHz | 32 MBps |
| VL-bus | 32 bits | 25 MHz | 100 MBps |
| VL-bus | 32 bits | 33 MHz | 132 MBps |
| PCI | 32 bits | 33 MHz | 132 MBps |
| PCI | 64 bits | 33 MHz | 264 MBps |
| PCI | 64 bits | 66 MHz | 512 MBps |
| PCI | 64 bits | 133 MHz | 1 GBps |

From the table above, it is clear that the buses can be operated under different speed, either 33 Mhz or 66 Mhz.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having different frequencies, since the Examiner takes Official Notice that the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al, and providing Tai with two PCI buses having different frequencies only involves ordinary skill in the art.

Claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al. in view of Lucent Technologies.

With regard to claims 1-3, Lange discloses a system for interconnecting two or more computer bus architectures, comprising: a first bus segment (primary PCI bus 12, Figs. 2 and 4) to transmit data information; a first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) connected to the first bus segment (primary PCI bus 12, Figs. 2 and 4); a second bus segment (secondary PCI bus 14, Figs. 2 and 4) to transmit data information; a second half bridge circuit (127, Fig. 2, column 5, lines 45-55) connected to the first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) and the second bus segment (secondary PCI bus 14, Figs. 2 and 4) for transferring data information between the first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) and the

second bus segment (secondary PCI bus 14, Figs. 2 and 4). In addition, Lange et al. also discloses that the first half bridge segment (12) and the second half bridge segment (14) communicate with a high speed serial line protocol (see at least col. 5, lines 49-51). Note that the serial line protocol includes a plurality of signal lines or data paths, see at least Fig. 2.

However, Lange does not disclose that the signal lines (provided by serial line protocol, see at least col. 5, lines 49-51, and Fig. 2) are "scalable" depending on a bandwidth needed for a particular application. To define the term "scalable", Applicants cited page 10, lines 6-10 of originally filed specification, which states that "[a]lthough the present invention is described with reference to embodiments teaching four high speed serial data lines running between two half bridge circuits, the principles of the present invention are equally applicable to the addition or subtraction of high speed serial data lines depending upon the bandwidth needed between two half bridge circuits." See Appeal Brief, Summary of the Invention, last three lines.

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can

be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 126 and 127 on each side of the PCI bus segments of Lange, for the purpose of providing Lange with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs.

With regard to claims 5, 14, 23, Lange clearly discloses that the bridge (PCI bridge connected to PCI buses according to PCI specification) can have a bus width of either 32 bits or 64 bits. See at least column 3, lines 54-60. According to the PCI specification, PCI is operated at 33 MHz using a 32-bit-wide path; and the speed can be

increased from 33 MHz to 66 MHz and the bit count can be doubled to 64. Currently, PCI-X provides for 64-bit transfers at a speed of 133 MHz.

| Bus Type | Bus Width | Bus Speed | MB/sec |
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| VL-bus | 32 bits | 25 MHz | 100 MBps |
| VL-bus | 32 bits | 33 MHz | 132 MBps |
| PCI | 32 bits | 33 MHz | 132 MBps |
| PCI | 64 bits | 33 MHz | 264 MBps |
| PCI | 64 bits | 66 MHz | 512 MBps |
| PCI | 64 bits | 133 MHz | 1 GBps |

From the table above, it is clear that the buses can be operated under different speed, either 33 Mhz or 66 Mhz.

With regard to claims 7, 16, and 25, the ORT4622 half bridge includes field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and 4th paragraph. With regard to claims 8, 17, and 26, since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ (see page 6, lines 20-

26), it is clear that the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

With regard to claims 10-12, 14, 18, see discussion above.

With regard to claims 19-21, and 23, see discussion above.

Claims 6, 15, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al., 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26, and further in view of the following.

Lange et al., as discussed above, discloses the claimed invention. Lange et al. does not disclose that the bus operating frequencies of PCI bus (2) and PCI bus (4) may be substantially the same. However, the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tal. Tal discloses that the first PCI bus segment operates at a substantially same bus frequency as a bus frequency of said second PCI bus segment (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having substantially same frequencies, since the Examiner takes Official Notice that the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tal (see column 4, line 61 to column 5, line 5; column 6, lines 18-27); and therefore, providing Lange et al.

with two PCI buses having substantially same frequencies only involves ordinary skill in the art.

**(10) Response to Argument**

As stated in sections 7 and 8, the **only** issue at question is whether the serial channel comprising a plurality of data paths, as disclosed by the prior art, is "scalable depending on a bandwidth needed for a particular application."

With regard to the Tal 103 Rejection, Appellants argue that the serial channel provided by Lucent Technologies' ORT4622 half bridge comprising FPGAs (Field Programmable Arrays) is not "scalable." See Appeal Brief, pages 5 and 6. Note that on page 6, part B, the term "OWKPA" used by Appellants to refer to the Lucent Technologies' ORT4622 half bridge.

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ.

Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

With regard to the Lange 103 Rejection, Appellants argue that the serial channel provided by Lucent Technologies' ORT4622 half bridge comprising FPGAs (Field Programmable Arrays) is not "scalable." See Appeal Brief, pages 9-11. Note that on page 11, part F, the term "OWKPA" used by Appellants to refer to the Lucent Technologies' ORT4622 half bridge.

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half

bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

This examiner's answer contains a new ground of rejection set forth in section **(9)** above. Accordingly, appellant must within **TWO MONTHS** from the date of this answer exercise one of the following two options to avoid *sua sponte* **dismissal of the appeal** as to the claims subject to the new ground of rejection:

(1) **Reopen prosecution.** Request that prosecution be reopened before the primary examiner by filing a reply under 37 CFR 1.111 with or without amendment, affidavit or other evidence. Any amendment, affidavit or other evidence must be relevant to the new grounds of rejection. A request that complies with 37 CFR 41.39(b)(1) will be entered and considered. Any request that prosecution be reopened will be treated as a request to withdraw the appeal.

(2) **Maintain appeal.** Request that the appeal be maintained by filing a reply brief as set forth in 37 CFR 41.41. Such a reply brief must address each new ground of rejection as set forth in 37 CFR 41.37(c)(1)(vii) and should be in compliance with the other requirements of 37 CFR 41.37(c). If a reply brief filed pursuant to 37 CFR 41.39(b)(2) is accompanied by any amendment, affidavit or other evidence, it shall be

treated as a request that prosecution be reopened before the primary examiner under 37 CFR 41.39(b)(1).

Extensions of time under 37 CFR 1.136(a) are not applicable to the TWO MONTH time period set forth above. See 37 CFR 1.136(b) for extensions of time to reply for patent applications and 37 CFR 1.550(c) for extensions of time to reply for ex parte reexamination proceedings.

Respectfully submitted,

Khanh Dang

**A Technology Center Director or designee must personally approve the new ground(s) of rejection set forth in section (9) above by signing below:**

PETER WONG, DIRECTOR
TECHNOLOGY CENTER 2100

Conferees:

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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